WHAT IS CLAIMED IS:

1. A wafer comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer;

said second portions comprise first dummy structures, said first dummy structures comprise a first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from said conductive layer.

2. The wafer of claim 1, wherein the isolation regions are shallow trench isolation regions.

3. The wafer of claim 1, wherein said conductive layer comprises polysilicon.

4. The wafer of claim 1, wherein said active layer comprises doped silicon.

5. The wafer of claim 1, further comprising an interconnect layer formed over said conductive layer.

6. The wafer of claim 5, wherein said interconnect layer comprises a metal.

7. The wafer of claim 1, wherein said third portion does not contain said active layer.

8. The wafer of claim 7, further comprising a silicon electrode contacting an isolation region.

9. The wafer of claim 1, wherein said second portion does not contain said conductive layer.

10. The wafer of claim 1, wherein said gate dielectric capacitor is a transistor.

11. A method of measuring gate dielectric thickness of a gate dielectric capacitor comprising:

providing a wafer comprising a plurality of gate dielectric capacitors, a plurality of first dummy structures, and a plurality of second dummy structures formed on said wafer;

measuring the capacitance of one of said gate dielectric capacitors;

measuring the capacitance of one of said first dummy structures;

measuring the capacitance of one of said second dummy structures;

subtracting the capacitances of said first dummy structure and said second dummy structure from the capacitance of said gate dielectric capacitor to obtain a capacitance difference; and

determining the gate dielectric thickness from said capacitance difference.

12. The method according to claim 11, wherein said wafer comprises a base layer, an active layer formed on said base layer, a gate dielectric layer formed on said active layer, a conductive layer formed on said gate dielectric layer, and a plurality of isolation regions.

13. The method according to claim 12, wherein said gate dielectric capacitors comprise a first electrode layer formed from said active layer; an insulating layer formed from said gate dielectric layer, and a second electrode formed from said conductive layer;

said first dummy structures comprise a first electrode layer formed from said active layer, and an insulating layer formed from said gate dielectric layer; and

said second dummy structures comprise an insulating layer formed from said isolation region, and a second electrode formed from said conductive layer.

14. The method according to claim 12, wherein said wafer further comprises an intermetal dielectric layer formed on said conductive layer.

15. The method according to claim 14, wherein said wafer further comprises an interconnect layer formed on said intermetal dielectric layer.

16. The method according to claim 12, wherein said active layer comprises doped silicon.

17. The method according to claim 12, wherein said conductive layer comprises polysilicon.

18. A method of manufacturing a wafer comprising a plurality of gate dielectric capacitors, first dummy structures, and second dummy structures, the method comprising the steps of:

providing a wafer comprising a base layer, an active layer formed on said base layer, a gate dielectric layer formed on said active layer, a plurality of isolation regions formed on said wafer, and a conductive layer formed on said gate dielectric layer and said isolation regions;

removing portions of said conductive layer where said first dummy structures are formed;

forming an intermetal dielectric layer over said conductive layer;

forming openings in said intermetal dielectric layer to expose said conductive layer, in a region where said gate dielectric capacitors are formed; said isolation region, in a region where said first dummy structures are formed; and the conductive layer, in a region where said second dummy structures are formed; and

forming an interconnect layer over said intermetal dielectric layer, said interconnect layer filling said openings in the intermetal dielectric layer.

19. The method according to claim 18, wherein said isolation regions comprise shallow trench isolation structures.

20. The method according to claim 18, wherein said conductive layer comprises polysilicon.